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Reliability-Oriented Design of Modular Multilevel Converters for Medium-Voltage STATCOM

João Victor Matos Farias, Allan Fagner Cupertino, *Member, IEEE,* Victor de Nazareth Ferreira, *Student Member, IEEE,* Heverton Augusto Pereira, *Member, IEEE,* Seleme Isaac Seleme Junior, Remus Teodorescu, *Fellow, IEEE*

***Abstract*—Modular Multilevel Converters (MMC) are complex systems, composed of many elements, and exposed to critical load demands in some cases. Thereby, a detailed design of its components is of preeminent importance to achieve a high system-level reliability. However, the high number of devices challenges the trade-off between cost and reliability. This work, introduces a reliability-oriented design methodology, based on the cost to achieve a pre-defined unreliability level (U_x). A flowchart presents the main steps of the process, including the mission profile definition, selection of power devices, thermal modeling, reliability modeling and the reliability-oriented selection. To evaluate the proposed methodology, a case study considering 17 MVA/13.8kV MMC-STATCOM with a real mission profile data is conducted. A $U_x - cost$ map is introduced to compare various design solutions, based on power devices of different voltage classes and current capabilities.**

***Index Terms*—MMC-STATCOM, Power Devices, Lifetime, Reliability-Oriented Design.**

I. Introduction

THE modular multilevel converter (MMC) has become an attractive topology for applications as HVDC Systems and STATCOMs [1]. The MMC topologies present a high number of low voltage bridges in cascaded connection, aiming to achieve a high voltage capability. Therefore, the MMC has more components than the traditional multilevel topologies [2]. In addition to higher costs, the increased number of components can affect significantly the system-level reliability of MMC [3], [4].

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J. V. M. Farias is with the Graduate program in Electrical Engineering, Federal Center for Technological Education of Minas Gerais, Belo Horizonte, MG, 30510-000 Brazil (Corresponding author: e-mail:joaofariasgv.jvmf@gmail.com).

A. F. Cupertino and V. N. Ferreira are with the Graduate Program in Electrical Engineering, Federal University of Minas Gerais, Belo Horizonte, MG, 31270-901 Brazil. A. F. Cupertino is also with the Department of Materials Engineering, Federal Center for Technological Education of Minas Gerais, Belo Horizonte, MG, 30421-169 Brazil (e-mail: afcupertino@ieee.org, vnferreira89@gmail.com).

H. A. Pereira is with the Department of Electrical Engineering, Universidade Federal de Viçosa, Viçosa, MG, 36570-900 Brazil (e-mail: heverton.pereira@ufv.br).

S. I. Seleme Junior is with the Department of Electrical Engineering, Federal University of Minas Gerais, Belo Horizonte, MG, 31270-901 Brazil (e-mail: seleme@cpdee.ufmg.br).

R. Teodorescu is with the Department of Energy Technology, Aalborg University 9220 Aalborg, Denmark (e-mail: ret@et.aau.dk).

The design for reliability (DFR) is a potential solution to increase the reliability of complex systems [5]. In this approach a well detailed design is conducted, aiming at reducing the wear-out failure probability of power devices. Some research efforts focused on the estimation of the MMC lifetime are identified in the literature [6]–[9]. Reference [6] presents a lifetime estimation procedure for MMC power modules based on physics of failure (PoF) models and mission profile, considering a 18 MW HVDC station. Reference [7] proposes an algorithm for fast thermal simulation of MMC and also estimates the power modules lifetime. In [8], the most commonly-used analytical lifetime models of insulated-gate bipolar transistor (IGBT) devices are compared, considering a 30 MW MMC-HVDC application with 6.5 kV IGBT modules. Reference [9] addresses the estimation of lifetime that compares two IGBT solutions with differently rated current levels. The results indicate a lower temperature in devices with higher current capability, increasing the converter lifetime.

In addition to the current level, the varied voltage classes of silicon-based power semiconductor devices, also challenges the MMC design [10]. Thereby, some studies define the optimum semiconductor blocking voltage to be used for different power levels. According to [10], 1.2 kV or 1.7 kV IGBT power modules are most suitable for 1 MVA systems to interface medium-voltage (MV) grids, considering only the power device efficiency. Reference [11] indicates that when the cost of transmitted power per cell unit and the penalties for the losses are taken into account, the 4.5 kV IGBT modules show the best performance for HVDC transmission for rated powers below of 900-1000 MW. Additionally, for values above 1050 MW, the cell designed with 6.5 kV IGBTs proved to be more attractive. Finally, reference [12] compares 5 designs by employing different IGBT voltage classes for a 5 MVA MMC based battery energy storage system. The results indicate that the 1.7 kV modules lead to the lowest cost, while 3.3 kV results in the lowest losses. Nevertheless, a reliability-oriented design methodology, including the design complexities of MMC converters, stills missing in technical literature.

This paper proposes a reliability-oriented design to obtain the best MMC solution, based on the trade-off between cost and system-level reliability. The unreliability level U_x is presented as a new reliability indicator to evaluate the probability of one failure in the converter for a given time. Moreover, the $U_x - cost$ map is introduced as a tool to compare different

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designs with respect to the unreliability requirement and cost. The methodology is exemplified through a 17 MVA/13.8 kV MMC-STATCOM case study.

This paper is outlined as follows. Section II performs the main parameter design of the MMC-STATCOM and presents the reliability-oriented design method. Section III presents the case study based on a real mission profile. The obtained simulation results are discussed in Section IV. Finally, Section V draws the conclusion of this work.

II. METHODOLOGY

A. MMC-STATCOM Design

The circuit of a three-phase MMC in double-star connection is illustrated in Fig. 1. The converter is connected to the main grid through a three-phase transformer, represented by resistive-inductive grid impedance R_g and L_g. Each MMC phase has two arms composed of a series-connected arm inductor L_{arm} and N chopper cells. These cells consist of two IGBTs S_1 and S_2 and two antiparallel connected diodes D_1 and D_2, an energy storage capacitor C. There is usually a switch S_T in parallel with the cell bypassing it in case of failures.

The complete control strategy used is based on reference [9], which employs the following controls: grid current control, circulating current control and individual balancing control. The grid current control is responsible for controlling the reactive power injected by the converter into the grid. Furthermore, the circulating current control reduces the current harmonics and inserts damping in the converter dynamic response. Finally, the individual balancing control is used to guarantee the voltage balance of the cell capacitors, since the phase-shift pulse width modulation (PS-PWM) method is employed. The modulation strategy employed does not influence the results presented in this work.

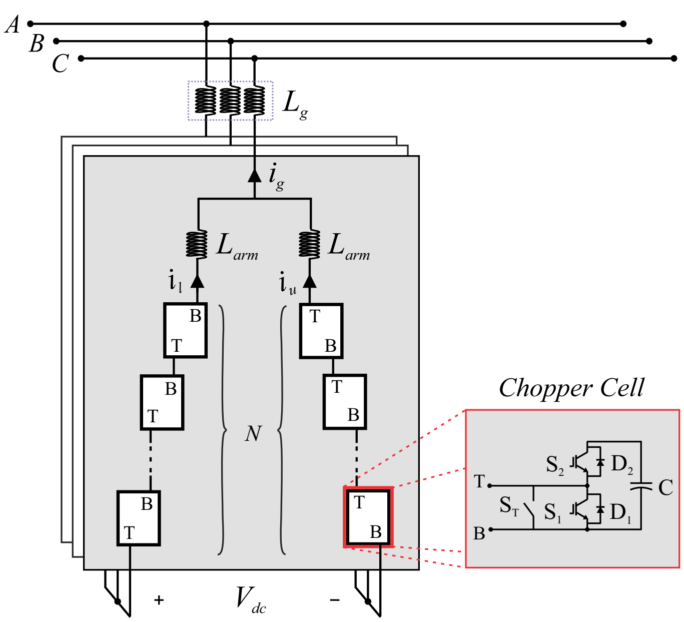

Fig. 1. Schematic of the three-phase MMC-STATCOM.

In this work, a MMC-STATCOM with rated power (S_n) of 17 MVA and line voltage (V_g) of 13.8 kV at the point of common coupling (PCC) is considered. The minimum value of the dc-link voltage can be approximated by [13]:

$$V_{dc} = \frac{2\sqrt{2}}{0.87\sqrt{3}} \frac{V_s}{\lambda m_{max}}, \tag{1}$$

where V_s is the line voltage synthesized by the STATCOM and λm_{max} is the maximum modulation index. According to [13], $V_s \approx 1.2V_g$. Furthermore, the modulation with the injection of $1/6$ of third harmonic reaches $\lambda m_{max} = 1.15$. Therefore, the approximate value of the effective dc-link voltage is $V_{dc} = 28$ kV.

The rated current of the power devices is defined by the MMC arm current. Due to symmetry, only the upper arm current is verified. The maximum and rms upper arm current is defined by [14]:

$$max(i_u) = \widehat{I}_n \left(\frac{1}{2} + \frac{\lambda m_{max}}{4} \right), \tag{2}$$

$$i_{u,rms} = \frac{\widehat{I}_n}{2} \sqrt{\frac{(\lambda m_{max})^2}{4} + \frac{1}{2}}, \tag{3}$$

where the nominal grid current $\widehat{I}_n$ is given by:

$$\widehat{I}_n = \frac{\sqrt{2}}{\sqrt{3}} \frac{S_n}{V_g}. \tag{4}$$

Thus, the $max\ (i_u) = 788$ A and $i_{u,rms} = 456$ A.

The number of cells is determined by:

$$N = \frac{1}{f_{us}} \frac{V_{dc}}{V_{svc}}, \tag{5}$$

where f_{us} is the ratio between the reference voltage of cells v^*_{sm} and the semiconductor device voltage class V_{svc}. The maximum recommended nominal voltage for semiconductor devices are approximately 63% of V_{svc} [15]. Assuming a cell capacitor voltage ripple of up to 10%, $f_{us} = 0.5$ is employed.

The cell capacitance can be designed based on the converter energy storage requirements. According to [16], the minimum cell capacitance is given by:

$$C_{cell} = \frac{N S_n W_{conv}}{3V_{dc}^2}, \tag{6}$$

where W_{conv} is the required energy storage per MVA. The minimum required value of W_{conv} is approximately 40 kJ/MVA, as defined in [17].

The number of cells and the capacitance are defined according to the blocking voltage of the semiconductor devices. Thus, a high number of cells increases the number of levels in the voltage output and reduces the size of the arm inductors due to the lower harmonic content in the output voltage and current [18]. The arm inductor is able to prevent the resonant frequency and limit the arm current during faults [19]. Therefore, the arm inductors are designed to satisfy the above constraint and limit the total harmonic distortion (THD)

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in output current i_g to 5% [12], [18]. The grid impedance is considered unchanged.

Based on the Eqs. (1)-(6), the main circuit parameters of the designed MMC-STATCOM are presented in Table I. As observed, IGBTs with blocking voltage capability range between 1.7 kV and 6.5 kV are considered.

TABLE I
MAIN PARAMETERS OF THE MMC-STATCOM FOR FOUR BLOCKING VOLTAGES: 1.7 KV, 3.3 KV, 4.5 KV AND 6.5 KV.

Parameters		MMC specifications			
		I	II	III	IV
N		33	17	13	9
V_{dc}	(kV)	28	28	28	28
V_{svc}	(kV)	1.7	3.3	4.5	6.5
V^*_{cell}	(kV)	0.85	1.65	2.15	3.11
C_{cell}	(mF)	9.54	4.92	3.76	2.61
L_{arm}	(mH)	4.46	8.70	11.82	17.08
L_g	(mH)	1.5	1.5	1.5	1.5
f_{sw}	(Hz)	210	210	210	210
f_{sample}	(kHz)	13.86	7.14	5.46	3.78

B. Reliability-Oriented Design

The design and selection of power electronics components demand the consideration of some factors, such as power losses, cost and the application unreliability requirement. Based on the DFR process [5], the reliability-oriented design illustrated in Fig. 2 presents the benchmarking and selection methodology for the semiconductor devices.

1) First Stage: Firstly, the mission profile is defined for the considered application. Measurements of reactive power (Q^*) and ambient temperature (T_a) mission profiles are employed in order to define the system operating condition. The most appropriate power devices can be selected according to the power rating, voltage and current levels.

2) Thermal Modeling: The power losses model employed is based on a look-up table of losses for each semiconductor device. As observed, the junction to case thermal impedance Z_{j-c} combines Cauer and Foster thermal networks to provide the best features of both models [20]. The case to heatsink impedance Z_{c-h} is represented by a thermal resistance. Moreover, the heatsink and cooling system, Z_{h-a}, are employed in order to ensure the operation of the power devices at the safety limit (e.g., T_j below 150 °C). The heatsink impedance present a parallel connection of the thermal resistance R_{h-f} and the capacitance C_{h-f} and can be estimated through the simplified methodology proposed in [21]:

$$R_{h-f} = \frac{d_h}{\lambda_h A_h}, \tag{7}$$

$$C_{h-f} = c_h \rho_h d_h A_h, \tag{8}$$

where d_h is the heatsink thickness, λ_h is the thermal conductivity of the heatsink material, A_h is the heatsink surface area, c_h is the specific heat capacity and ρ_h is the material density.

The cooling system is coupled to improve the heat exchange from the heatsink to the ambient, described by R_{f-a}. This thermal resistance presents a series connection to the heatsink and can be calculated by [21]:

$$R_{f-a} = \frac{1}{f_c A_h}, \tag{9}$$

where f_c is the fluid flow convection coefficient [22].

3) Reliability Modeling: The thermal cycling causes cyclic thermo-mechanical stresses in all joints and components of the power modules, which leads to wear-out failure in the device. Since the lifetime consumption (LC) evaluation is reached by the regular series of temperature profiles with constant average value, a rainflow counting method is employed [6] in order to provide the average temperature $T_{[j,c]m}$, cycle amplitude $\Delta T_{[j,c]}$ and heating time $t_{[j,c]on}$. Thereby, the LC is obtained by using the Palmgren-Miner rule [23]:

$$LC = \sum_i \frac{n_i}{N_{f,i}}, \tag{10}$$

where n_i is the number of cycles obtained from rainflow algorithm and N_f is the number of cycles to wear-out failure obtained for each stress condition. In this work, N_f is evaluated through the ABB Hi-Pak IGBT power module lifetime model [24]. This model analyzes N_f in all critical joints (bond wire, base plate solder and chip solder) for each diode and IGBT of the modules using the 10% failure rate approach (B_{10} lifetime).

The LC of the power device obtained from Eq. (10) can be considered as an ideal case, where all the power devices fail at the same time. Since the power devices could present variations in their parameters due to the manufacturing process and stress variation [25], this approach is not appropriate, especially for the large number of cells in the MMC. Thus, lifetime is usually expressed in terms of statistical values rather than a constant value. Therefore, a statistical analysis based on Monte-Carlo simulation is employed [26]. This analysis transforms the dynamic values obtained by rainflow algorithm into equivalent static values, $T'_{[j,c]m}$, $\Delta T'_{j,c}$ and t'_{on} [25]. These equivalent static parameters must provide the same LC, even as when the dynamic values are employed in the Eq. (10).

Once the equivalent static values have been obtained, a variation of 5% is applied in these parameters and in the lifetime model used. Afterward, the Monte-Carlo simulation of 10000 samples is performed. Then, the lifetime distribution obtained from Monte Carlo simulation is fitted with the Weibull PDF $f(x)$ [25], given by:

$$f(x) = \frac{\beta}{\eta^\beta} x^{(\beta-1)} exp\left[-\left(\frac{x}{\eta}\right)^\beta\right], \tag{11}$$

where β is the shape parameter, η is the scale parameter, and x is the operation time. The cumulative density function (CDF), also called unreliability function $F(x)$, represents the proportion of population failure, according to the time obtained through the integral of PDF, given as:

$$F(x) = \int_0^x f(x)dx, \tag{12}$$

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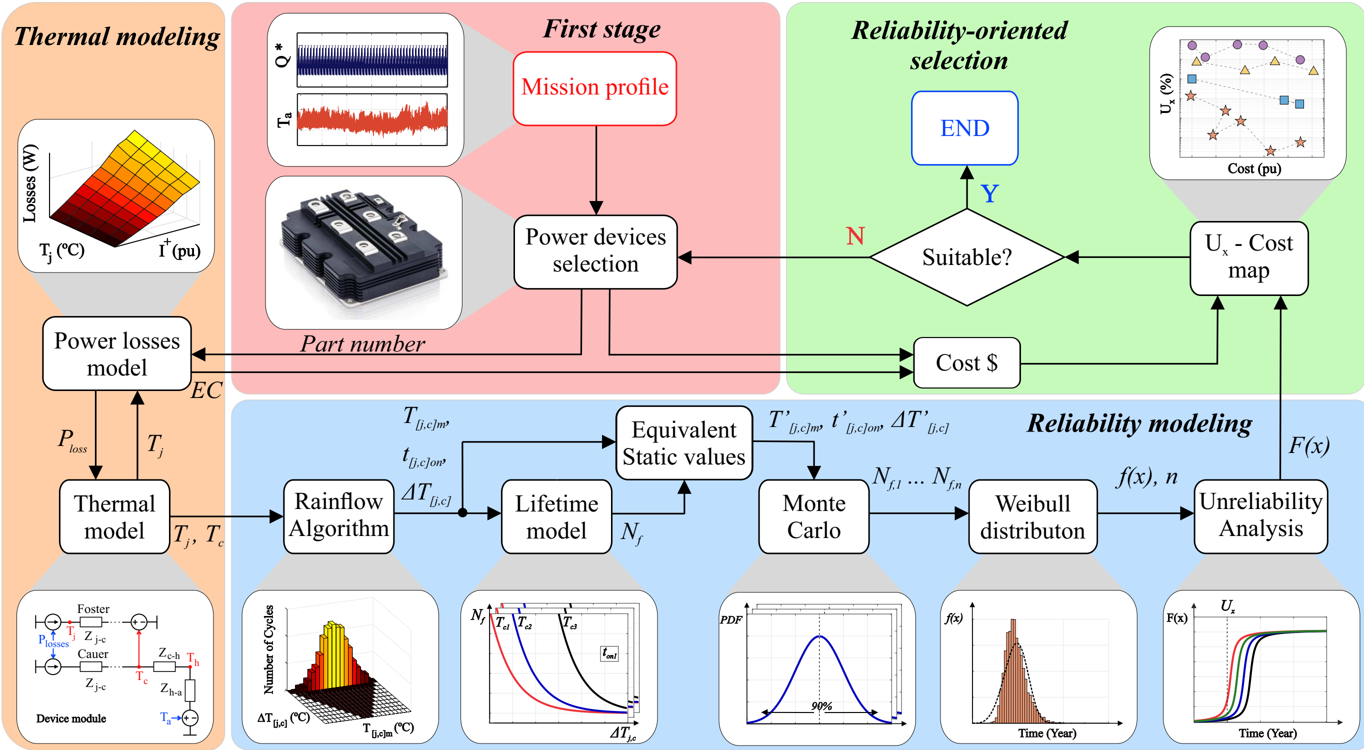

Fig. 2. Flowchart for the reliability-oriented design of power devices.

Since only the reliability of the power devices is taken into account in this study (i.e., S_1, S_2, D_1 and D_2), the unreliability function for each MMC chopper cell can be calculated as:

$$F_{cell}(x) = 1 - \prod_{i=1}^{4} (1 - F_{Comp(i)}(x)), \tag{13}$$

where $F_{Comp(i)}(x)$ is the unreliability function of each power device. Assuming that the converter presents 6 identical arms with N independent and identical cells per arm, the MMC system level unreliability function can be evaluated as follows:

$$F_{MMC}(x) = 1 - \prod_{n=1}^{6N} (1 - F_{cell(n)}(x)). \tag{14}$$

4) Reliability-Oriented Selection: The reliability studies on the converters are appropriate for the maintenance schedule and the prediction of the power devices' lifetime [27]. Since the beginning of the transitioning from the reliability books to PoF in power electronics [28], the converter lifetime has been expressed in N_f. Recently, the B_x factor was introduced, and translated the N_f into the number of years where $x\%$ of the devices fail [24]. Even though it is consolidated among the reliability researchers and designers, it is still quite confusing for industry engineers, which are responsible for the selection of converters.

In order to simplify this communication between reliability design engineers and industry engineers, this work introduces the unreliability level U_x as a new reliability indicator. Basically, for a given lifetime target x, the probability of failure is evaluated through the system unreliability. In other words, U_x is the probability of one failure for a given time, which can be measured considering the durability or the maintenance schedule of the converter. In addition, the $U_x - cost$ map is introduced as a tool to compare different designs with respect to the unreliability requirement and the overall cost. Finally, the most suitable design will find the lifetime target with the lowest cost.

Regarding the overall cost of each design, the figure of merit employed includes the capital expenditure (CAPEX) and operational expenditure (OPEX). The CAPEX is mainly related to investment in power electronics (e.g., semiconductor devices, controls, cabinets), which is dominant in the initial investment of the converter [12]. Thus, the cost of power electronics is considered as follows:

$$K_{sw} = K_c N_{semi} V_{svc} I_{svc}, \tag{15}$$

where N_{semi} is the number of semiconductor devices and I_{svc} is the rated device current. Based on installed switching power, $K_c = 3.5$ €/kVA is employed [12].

Moreover, the costs of passive elements should be included. According to [29], the cost of the cell capacitors K_{cap} are 150 €/kJ. Furthermore, the cost of the magnetic devices K_{mag} in euros can be estimated by [12], [29]:

$$K_{mag} = 4000 N_{mag} + 723000 A_p, \tag{16}$$

where N_{mag} is the number of inductors and A_p is the total area product (in m^4) of the cores of all inductors. The area product of a single magnetic core is the product of the winding-window area and the core cross sectional area.

Finally, the capital expenditure is given by:

$$CAPEX = K_{sw} + K_{mag} + K_{cap}. \tag{17}$$

Moreover, the OPEX is mainly associated to the semiconductor conduction and switching losses [30]. Therefore, the operational expenditure of the converter is considered as follows:

$$OPEX = K_o E_c, \tag{18}$$

where K_o is the price per kilowatt-hour and E_c is energy consumption of the converter. Based on loss penalty for transmission system, $K_o = 0.11$ €/kWh an one year is employed [11]. Thus, the overall cost is given by:

$$Cost = CAPEX + OPEX, \tag{19}$$

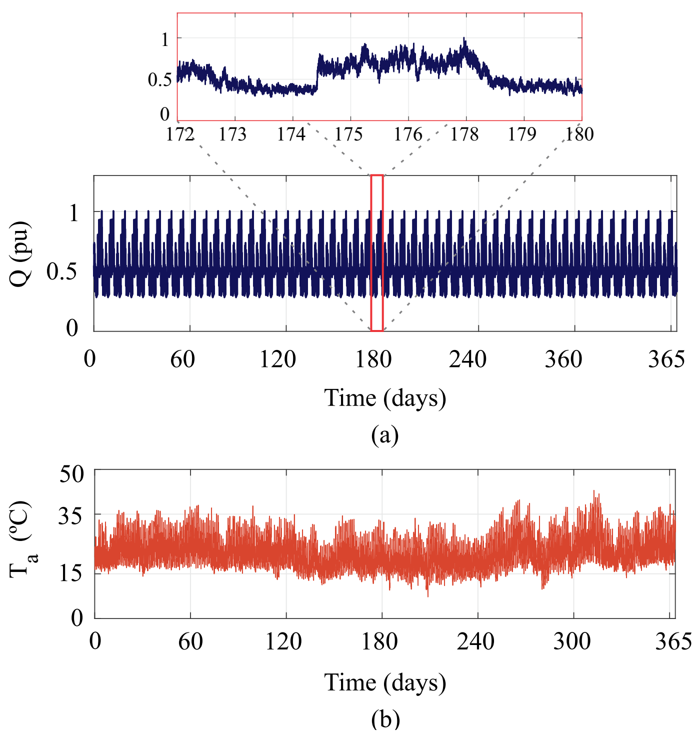

Fig. 3. Mission profiles: (a) Reactive Power; (b) Ambient Temperature.

III. Case Study

Based on the topology presented in Fig. 1, the simulations were performed using the *PLECS* and *MATLAB* software systems, aiming to estimate the lifetime, energy losses and cost of each design. Fig. 3 (a) shows the mission profile based on the reactive power measurements obtained from a factory in one week. In this work, this profile was replicated for a year. Furthermore, the one-year ambient temperature profile is illustrated in Fig. 3 (b). The data were collected from the southeastern Brazil with a sampling time of 1 second.

Table II shows the part numbers evaluated in this work. As observed, all the commercial available ABB Hi-pak IGBT solutions with rated current from 750 A to 1600 A are selected. Implementations based on parallel connection are also employed. All cells are considered identical. As a result, 18 different implementations are evaluated. Four base cases (i.e., C_1, C_4, C_{10}, C_{14}) are considered, which are the lowest rated current devices for each voltage class.

TABLE II
ABB Semiconductors Devices Solutions.

Voltage (V)	Current (A)	Part Number	Case
1700	800	5SND 0800M170100	C_1
	2x800	5SND 0800M170100	C_2
	1600	5SNA 1600N170100	C_3
3300	800	5SNA 0800N330100	C_4
	2x500	5SND 0500N330300	C_5
	1000	5SNA 1000N330300	C_6
	1200	5SNA 1200E330100	C_7
	1500	5SNA 1500E330305	C_8
	2x800	5SNA 0800N330100	C_9
4500	800	5SNA 0800J450300	C_{10}
	1200	5SNA 1200G450300	C_{11}
	2x650	5SNA 0650J450300	C_{12}
	2x800	5SNA 0800J450300	C_{13}
6500	750	5SNA 0750G650300	C_{14}
	2x400	5SNA 0400J650100	C_{15}
	2x500	5SNA 0500J650300	C_{16}
	2x600	5SNA 0600G650100	C_{17}
	2x750	5SNA 0750G650300	C_{18}

The data used in the power losses and thermal impedances Z_{j-c} and Z_{c-h} are extracted from the datasheets. The heatsink parameters are estimated based on the methodology proposed in [21]. The values of R_{h-f} and C_{h-f} vary according to the area and thickness of the heatsink. In this work, the area is considered to be equal to the total area of the power module, from the device datasheet. Furthermore, an aluminum heatsink with 3 cm of thickness are employed [21]. Regarding water-cooling system [22], the R_{f-a} values were determined through simulation in order to maintain the maximum junction and case temperature below 130 °C and 120 °C, respectively.

The A_p and E_{cap} values are given in Table III. The MMC presents 6 inductors and the capacitive energy stored is 40 kJ/MVA for all cases.

The converter lifetime target is defined as 10 years of operation. Thus, $E_{c_{10}}$ is the converter energy consumption for 10 years of operation. Finally, U_{10} is applied for reliability-oriented design, which means the probability of converter failure in 10 years of operation.

TABLE III
Cell Capacitors and Magnetic Devices Parameters for Cost Design.

Parameters		MMC specifications			
		I	II	III	IV
A_p	($m^4 \cdot 10^{-3}$)	20.05	39.11	53.08	76.70
E_{cap}	(kJ)	680	680	680	680

IV. Results and Discussion

Initially, the power losses, including conduction and switching losses, of a power module device are obtained. Fig 4

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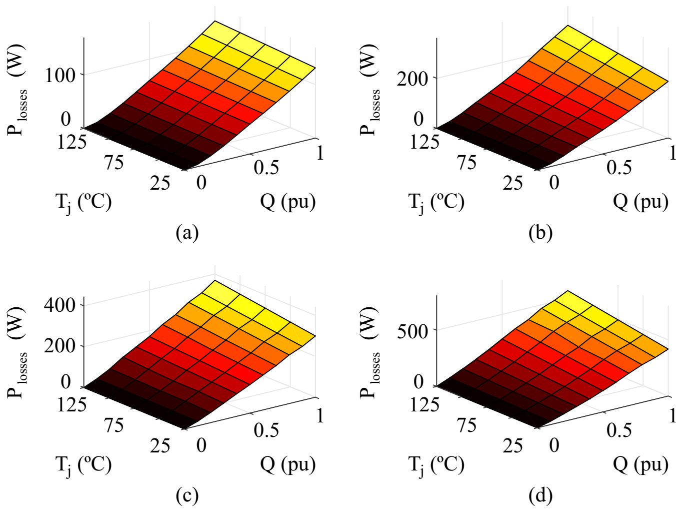

Fig. 4. Power losses of a power module device for the base cases: (a) C_1; (b) C_4; (c) C_{10}; (d) C_{14}.

shows the look-up table of losses for the base cases based on manufacturer's datasheet. As observed, an increase in power rated or junction temperature in the power devices, cause an increase in power losses. Moreover, power modules with higher blocking voltages present higher power losses.

The water flow convection coefficient is adjusted in order to maintain the average heatsink temperature close to 60 °C, for the base cases. Table IV presents the parameters of the heatsinks and cooling system. As observed, the resistance and capacitance parameters of the heatsink have approximate values due to the similar dimensions of the power modules. Therefore, a lower thermal resistance in the cooling system is required for the power modules that present higher losses. The solutions with different rated current present the same heatsink and cooling system parameters given in Table IV, according to the blocking voltage.

TABLE IV
HEATSINK AND COOLING SYSTEM PARAMETERS FOR POWER MODULES OF THE BASE CASES.

Parameters		C_1	C_4	C_{10}	C_{14}
R_{h-f}	(°C/kW)	6.9	6.9	6.9	4.7
C_{h-f}	(J/°C)	1327	1327	1327	1939
R_{f-a}	(°C/kW)	142.8	70.2	52.1	36.1

The MMC-STATCOM power losses are evaluated for different reactive power levels. The solutions C_1 and C_3 are illustrated in Fig. 5 (a). As observed, the power losses decrease when the rated current of the power module increases. However, the device with lower current rate C_6 presents lower losses than the solution C_7, as shown in Fig. 5 (b). As noted, the increase of the current rate compared with the power losses of the device does not present a straightforward relation.

The thermal stresses in the junction temperature of the power devices are illustrated in Fig. 6. The temperature profile is analyzed for one week. As observed, the junction temperature variations are similar to the mission profile of Fig.

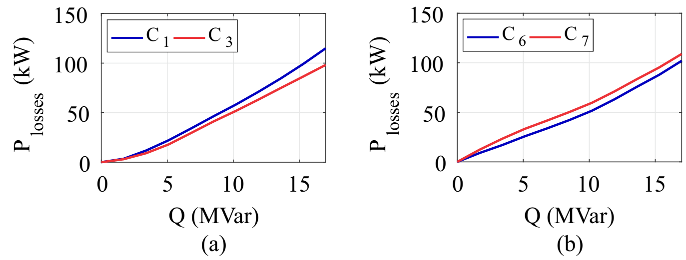

Fig. 5. Power losses in the MMC-STATCOM for different reactive power level, based on: (a) 1.7kV devices; (b) 3.3kV devices.

3 (a). Furthermore, the detail in Fig. 6 (a) shows that D_2 is the most stressed semiconductor device in the cells, since STATCOM operation is treated. The solution with the lowest rated current level (C_1) presents a thermal amplitude of 70.7 °C, approximately 18% higher than the C_3 solution. In addition, it is observed that the average temperature and its maximum instantaneous value increase. However, the maximum values are below 130 °C.

Since the thermal cycling is obtained, the rainflow algorithm and the lifetime model are applied. Figure 7 shows the life consumption (LC) in one year for all critical joints of the power devices. As observed, C_1 presents higher LC in all devices and joints. Moreover, the baseplate solder is the most damaging factor. Therefore, the Monte Carlo simulation considers this failure mechanism.

Therefore, the Weibull distribution PDF is obtained by employing the static values and the lifetime model into the Monte Carlo simulation with 10000 samples and 5% variation. For the sake of simplicity, only the lifetime distribution of D_2 device is presented. Fig. 8 shows the result obtained for the four base cases. The scale and shape parameters are shown for each base case. As observed, power devices with higher

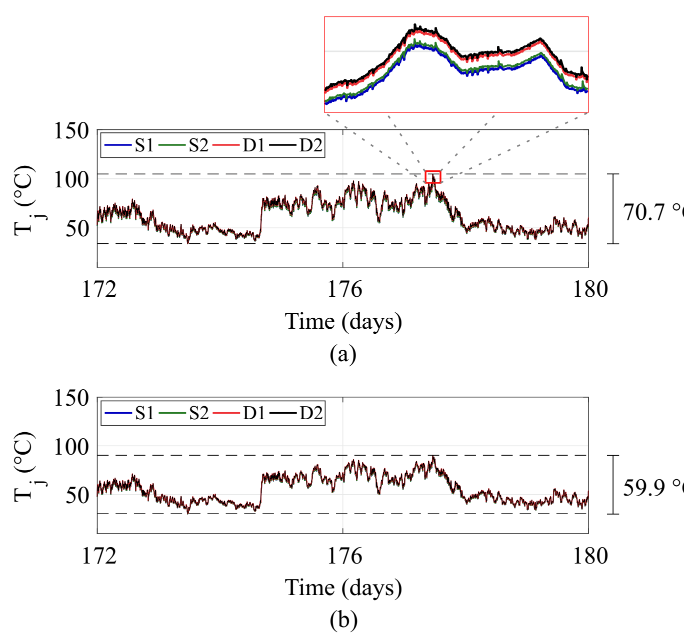

Fig. 6. Junction temperatures of the devices in a cell for two 1700V IGBT solutions: (a) C_1; (b) C_3.

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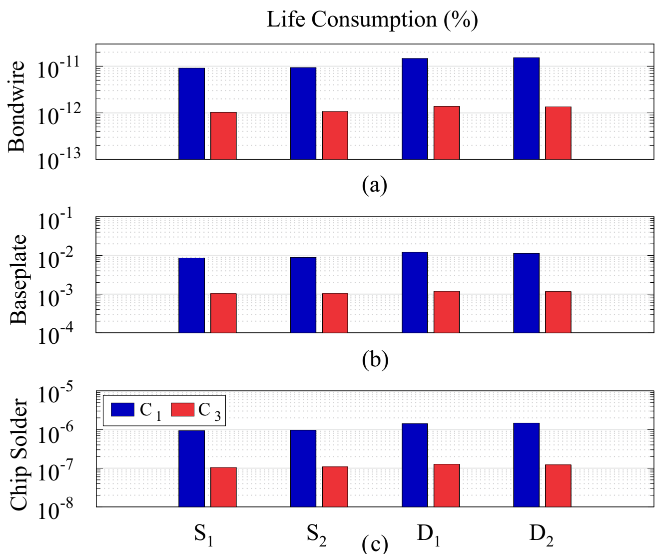

Fig. 7. Static life consumption for one year of power devices (semi-logarithmic scale): (a) Bondwire; (b) Baseplate; (c) Chip Solder.

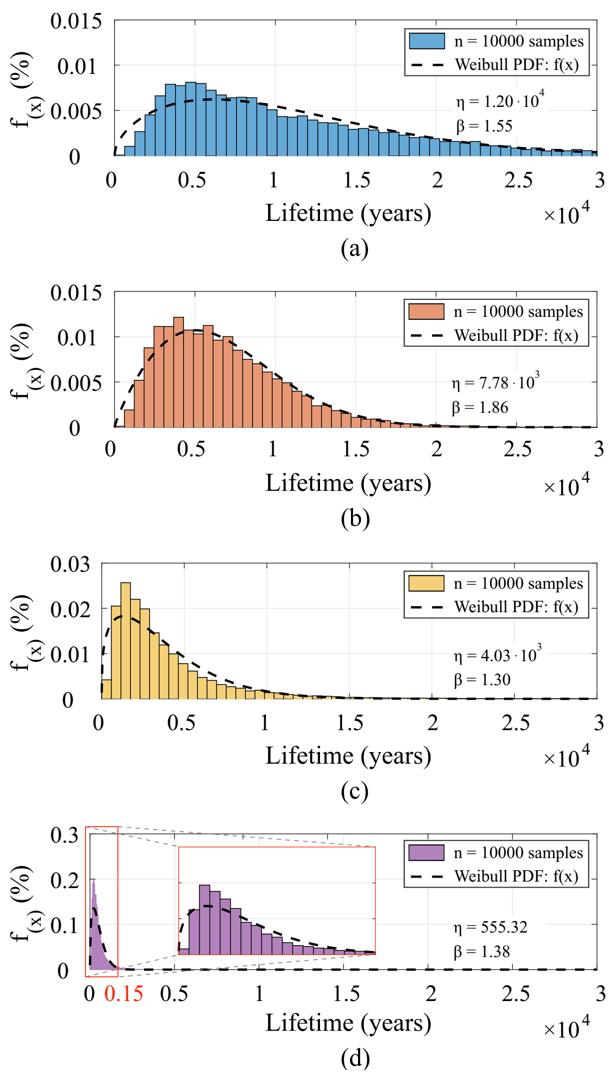

Fig. 8. Lifetime distribution (i.e., the Weibull PDF function) of the most stressed device D_2 for base cases: (a) C_1; (b) C_4; (c) C_{10}; (d) C_{14}.

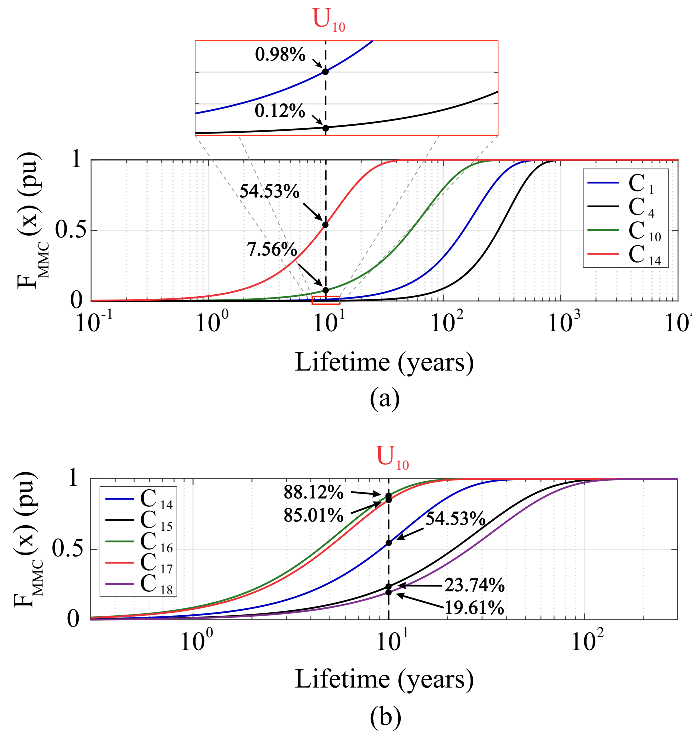

Fig. 9. MMC system level unreliability function (semi-logarithmic scale): (a) Power devices with the lowest rated current devices for each voltage class (b) Power devices with 6.5 kV blocking voltage.

blocking voltages present a lower scale parameter. Fig. 8 (c) and (d) show that the 4.5 kV and 6.5 kV voltage classes have more concentrated distribution due to higher thermal losses and stresses in the devices.

The previously lifetime analysis is based on component-level assessment. Eqs. (13) and (14) are used to obtain a MMC system level reliability assessment. Thus, the unreliability functions for the base cases are shown in Fig. 9 (a). Considering 10 years of operation, the U_{10} unreliability level is analyzed. As observed, the MMC based on the design C_4 presents the lowest failure probability of 0.12%, when power devices with similar rated current are compared. Furthermore, C_{14} has the highest probability of failure, 54.53%. Fig. 9 (b) illustrates the effect of increasing the rated current of semiconductor devices, considering the 6.5 kV voltage class. As observed, it can be concluded that the design with greater current capability C_{18} presents a failure probability of 19.61%, while C_{16} presents 88.12%.

Table V presents the results for all solutions proposed in this work. The energy consumption is given for 10 years of operation $E_{c_{10}}$, the values are given in per unit (pu) in the base of the 444.2 MWh per year. The cost is also presented in pu and its base value is 2.53 M€. Base values refer to the C_1 design. Moreover, the three best performances of each analysis are highlighted in Table V. As observed, the solution C_8 has the lowest U_{10} unreliability, whereas C_2 presents the lowest energy consumption and C_4, the lowest cost among the studied solutions.

Finally, Fig. 10 presents the $U_{10} - cost$ map. In order to exemplify the reliability-oriented design, two examples are

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TABLE V
COMPARISON OF THE PROPOSED DESIGNS.

Case	U_{10} (%)	E_{c10} (pu)	Cost (pu)
C_1	0.98	1	**1**
C_2	0.10	**0.77**	1.70
C_3	0.08	0.89	1.72
C_4	$11.78 \cdot 10^{-2}$	0.95	**0.99**
C_5	$2.22 \cdot 10^{-2}$	0.92	1.18
C_6	$\mathbf{0.11 \cdot 10^{-2}}$	0.90	1.17
C_7	$0.62 \cdot 10^{-2}$	1.06	1.39
C_8	$\mathbf{0.01 \cdot 10^{-2}}$	**0.83**	1.62
C_9	$\mathbf{0.09 \cdot 10^{-2}}$	**0.80**	1.71
C_{10}	7.56	1.05	1.05
C_{11}	2.78	1.01	1.43
C_{12}	15.24	1.05	1.54
C_{13}	4.91	0.97	1.81
C_{14}	54.53	1.10	**1.02**
C_{15}	23.74	0.97	1.04
C_{16}	88.12	1.17	1.28
C_{17}	85.01	1.12	1.46
C_{18}	19.61	0.98	1.72

considered, $U_{10} < 10\%$ and $U_{10} < 0.1\%$. As observed, the voltage class of 6.5 is not suitable for an unreliability level less than 10%. Furthermore, C_4 meets the requirement, with the lowest cost among the eligible designs. However, if the unreliability level is more restricted, for example, less than 0.1%, the only possible solutions are in the voltage classes of 1.7 kV and 3.3 kV. In this case, C_6 is the most attractive design.

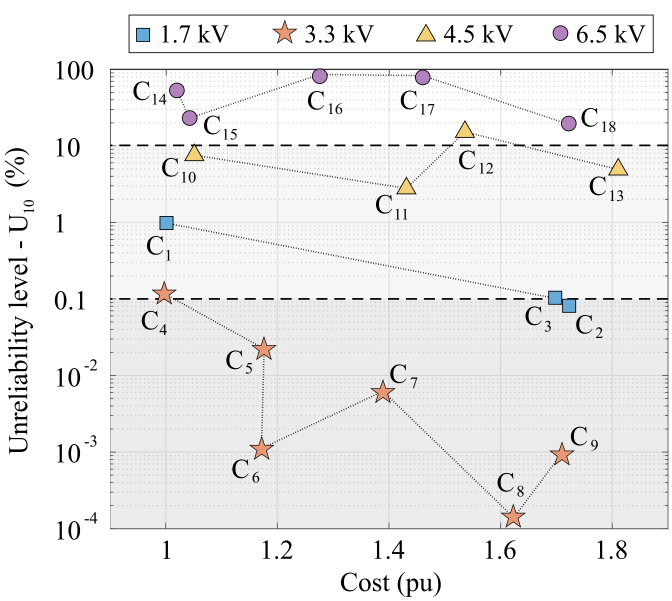

Fig. 10. U_{10} x $Cost$ map for the reliability-oriented design (semi-logarithmic scale).

In this work, U_{10} is employed because the expected operation time of the converter is 10 years. However, this analysis can be easily extended according to the target lifetime and the unreliability requirement of each application.

V. CONCLUSION

This work proposed a reliability-oriented design methodology for modular multilevel converter, based on wear-out failure events of power devices. For that, the unreliability level U_x is presented as a new reliability indicator to evaluate the probability of one failure in the converter for a specified time. The U_x x $Cost$ map allows the design engineer to select the most suitable power device according to the converter reliability requirement.

A 17 MVA/13.8 kV MMC-STATCOM case study is adopted. The simulation results indicate that the solutions based on 3.3 kV present the best U_{10} - cost trade-off, followed by the 1.7 kV devices. The high losses and thermal stresses indicate that the 6.5 kV devices are unsuitable for the proposed case study.

It is important to mention that the reliability-oriented design methodology proposed in this paper can be extended to other multilevel converters, semiconductor technologies, applications and cost methodologies.

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João Victor Matos Farias received the B.S. degree in electrical engineering from the Federal University of Viçosa (UFV), Brazil, in 2018. Currently, he is working toward the Master's degree in electrical engineering at the Federal Center of Technological Education of Minas Gerais (CEFET). His main research interests include modular multilevel converters, HVDC and STATCOM applications, electric drives and reliability of power converters.

Allan Fagner Cupertino (M'15) received the B.S. degree in electrical engineering from the Federal University of Viçosa (UFV) in 2013 receiving the President Bernardes Silver Medal. He received the M.S. degree in Electrical Engineering from the Federal University of Minas Gerais (UFMG). Since 2014 he has been with the Materials Engineering Department at the Federal Center of Technological Education of Minas Gerais (CEFET), teaching in the area of electric machines. Currently, he is working toward the Ph.D. project about the use of modular multilevel converters in STATCOM applications. His main research interests include renewable power generation systems, multifunctional inverters, modular multilevel converters and reliability of power electronic converters.

Victor de Nazareth Ferreira received the master degree in electrical engineering from the Federal University of Minas Gerais, Brazil, in 2016. He is a Research Assistant and is currently working toward the Doctor's degree in electrical engineering, in the Chair of Power Electronics, Kiel University, Germany. He has industry experience working as a Research and Development Engineer with medium-voltage converters. His current research and technical interests include reliability, power semiconductor devices, dc-dc, multilevel and modular converters.

Heverton Augusto Pereira (M'12) received the B.S. degree in electrical engineering from the Federal University of Viçosa (UFV), Brazil, in 2007, the M.Sc. degree in electrical engineering from the University of Campinas (UNICAMP), Brazil, in 2009 and the Ph.D. degree from the Federal University of Minas Gerais (UFMG), Brazil, in 2015. He was a guest Ph.D. from the Department of Energy Technology, Aalborg University, Denmark in 2014. He has been Adjunct Professor at the Electric Engineering Department, UFV, Brazil, since 2009. His main research interests includes: grid-connected converters for photovoltaic and wind power systems, HVDC/FACTS based on MMC.

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Seleme Isaac Seleme Junior received the B.S. degree in electrical engineering from the Escola Politecnica (USP), São Paulo, Brazil, in 1977, the M.S. degree in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1985, and the Ph.D. degree in control and automation from the Institut National Polytechnique de Grenoble (INPG), Grenoble, France, in 1994. He spent a sabatical leave with the Power Electronics Group, Univesity of California, Berkeley, in 2002. In 2015, he spent a sabatical leave with the Institut National Polytechnique de Toulouse, INP, France where he developed researches about decentralized control and capacitor voltage estimation techniques for modular multilevel converters. He is currently an Associate Professor with the Department of Electronic Engineering, Federal University of Minas Gerais, Belo Horizonte, Brazil. His main research interests include renewable energy systems, modular multilevel converters and nonlinear control applied in power converters.

Remus Teodorescu (F'12) received the Dipl.Ing. degree in electrical engineering from the Polytechnical University of Bucharest, Bucharest, Romania, in 1989, and the Ph.D. degree in power electronics from the University of Galati, Romania, in 1994. In 1998, he joined the Power Electronics Section, Department of Energy Technology, Aalborg University, Aalborg, Denmark, where he is currently a Full Professor. Since 2013, he has been a Visiting Professor with Chalmers University. His research interests include design and control of grid-connected converters for photovoltaic and wind power systems, HVDC/FACTS based on modular multilevel converters (MMC) and storage systems based on Li-ion battery technology including modular converters and active BMS.